The Specification has been amended to incorporate priority claims to previous applications.

Marked-up versions of the amendments to the application are shown on a separate set of pages attached hereto and entitled MARKED-UP VERSIONS SHOWING AMENDMENTS TO THE APPLICATION, which follows the signature page of this Response. On this set of pages, the insertions are underlined while the ~~deletions are struck through~~.

Response to Rejections

Applicant will treat all of the cited references as prior art for purposes of responding to the outstanding Office Action, but reserves the right to demonstrate his own prior invention at a later date. By focusing on specific references, claims and limitations, Applicant does not intend to imply an agreement with the Examiner's assertions with respect to other references, claims, and limitations.

As to Independent Claim 13

In the Office Action, the Examiner takes the position that the previously pending Claim 13 was anticipated by Buhler. Claim 13 had been amended previously so as to state that the gates of the first and third transistors are coupled together. The Examiner states in the Office Action that "since the first transistor and the third transistor are disposed on a single substrate, the gates of the first and third transistors are coupled together." It appears that the Examiner has interpreted the term "coupled" to mean that the gates are mechanically coupled together by being on the same substrate, Applicant intended to require a direct electrical coupling.

Claim 13 has now been amended to add additional language to further emphasize that the gate of the first transistor and the gate of the third transistor are directly tied to a single DC voltage. Independent Claim 13, as amended, now recites "wherein the gate of the first transistor and the gate of the third transistor are electrically coupled together to a same DC voltage." This limitation is clearly not taught or suggested by Buhler.

As shown in Fig. 2 of Buhler, Φ_{DR}, which is the signal applied at the gate of the first transistor, is a clock signal, and therefore the gate of the first transistor, according to Buhler, is not permanently connected to a DC voltage. The Examiner maintains that the gates of transistors M2 and M1 are coupled together to a DC voltage. A clock signal, however, is not a DC voltage but an AC voltage. Further, in Buhler, the two gates are not connected to the **same DC voltage**

as the gate of M1 is coupled to the clock signal Φ_{DR} (which is an alternating voltage) whereas M2 is coupled to the DC transfer gate voltage V_{tl} (see col. 3, lines 10 to 19).

Since Buhler does not teach the above-referenced limitations, Applicant respectfully submits that Claim 13 is not anticipated and should be allowable.

As to Dependent Claim 14-15 and 17

Claims 14-15 and 17 depend from Claim 13 and should likewise be allowable for at least the reasons set forth above with respect to Claim 13. These dependent claims also recite additional patentable distinctions over the cited art. For example, Claim 14 recites "wherein said gate of said first transistor is at a first voltage and said first electrode of said first transistor is at a second voltage, said second electrode of said first transistor being connected to said photosensitive element, said gate of said second transistor being connected to said third transistor."

CONCLUSION

In view of the foregoing remarks, Applicant submits that the application is in condition for allowance. If, however, issues remain which can potentially be resolved by telephone, the Examiner is invited to call the undersigned attorney of record at his direct dial number of (949) 721-6377.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 6/28/02

By: _____

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MARKED-UP VERSIONS SHOWING AMENDMENTS TO THE APPLICATION

In the Claims

13. (Four Times Amended) A pixel for imaging applications fabricated in a MOS technology, said pixel comprising:

photosensitive element and a first transistor having a gate and a first and second electrode and being in series with said photosensitive element, said first transistor and said photosensitive element thereby forming a first connection;

a second transistor having a gate, said second transistor being coupled to said first connection, thereby forming a second connection, and said second transistor being part of an amplifying circuit; and

a third transistor having a gate and having two electrodes, said third transistor being connected in said second connection between said first connection and said second transistor;

~~whereby~~ wherein the gate of the first transistor and the gate of the third transistor are electrically coupled together ~~and are both connected~~ to a same DC voltage.

14. (Previously Amended) The pixel as recited in Claim 13, wherein said gate of said first transistor is at a first voltage and said first electrode of said first transistor is at a second voltage, said second electrode of said first transistor being connected to said photosensitive element, said gate of said second transistor being connected to said third transistor.

15. (Previously Amended) The pixel as recited in Claim 14, wherein said gate of said first transistor is at said first voltage and wherein one of said electrodes of said third transistor is connected to said gate of said second transistor and the other of said electrodes is connected to said first connection.

17. (Amended) The pixel ~~is~~ as recited in Claim 13, wherein said gate of said first transistor is at a first voltage and said first electrode of said first transistor is at a second voltage, said second electrode of said first transistor being connected to said photosensitive element.